LISTING OF THE CLAIMS

The following Listing of the Claims replaces all previous listings of the claims within this application.

1. - 8. (canceled)

9. (previously amended) A microelectronic fabrication comprising:

a substrate; and

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns.

10. (canceled)

11. (original) The microelectronic fabrication of claim 9 wherein the microelectronic structure is selected from the group consisting of resistors, diodes, capacitors, bond pads and aggregates thereof.

12. (original) The microelectronic fabrication of claim 9 wherein the microelectronic structure comprises a capacitor electrically connected with a bond pad.

13. (original) The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed of a conductor material selected from the group consisting of non-magnetic metal, non-magnetic metal alloy, magnetic metal, magnetic metal alloy, doped polysilicon and polycide conductor materials, and laminates thereof.

14. (original) The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed in a geometric shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, an ellipse and a circle.

15. (previously amended) A microelectronic fabrication comprising:

a substrate;

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns; and

a bond wire bonded upon the microelectronic structure, wherein the bond wire has incorporated therein a minimum of one loop.

16. (original) A microelectronic fabrication comprising:

a substrate; and

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns, such as to attenuate eddy currents within the microelectronic structure.

17. (previously added) A microelectronic fabrication comprising:

a substrate;

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns; and

a bond wire bonded upon the microelectronic structure, wherein the bond wire has incorporated therein a plurality of loops.